Abstracts

Geometry and bias current optimization for SiGe HBT cascode low-noise amplifiers (2002 [RFIC])

Qingqing Liang, Guofu Niu, J.D. Cressler, S. Taylor and D.L. Harame. "Geometry and bias current optimization for SiGe HBT cascode low-noise amplifiers (2002 [RFIC])." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 407-410.

This work presents a new design methodology for inductively-degenerated cascode low-noise amplifiers using advanced epitaxial-base SiGe HBTs. Noise figure, gain, and IIP3 are calculated using calibrated linear circuit analysis and a Volterra series methodology as a function of the two major design variables: emitter geometry and biasing current. An optimum SiGe HBT LNA design point which balances input impedance match, high IIP3, noise figure, gain, and power consumption is obtained from calculated noise figure, gain, and IIP3 contours as a function of bias current and geometry. Simplified analytical expressions of IIP3, gain, and noise figure are presented to give additional insight. The optimum LNA design point for the 50 GHz SiGe HBT process technology under study yields a 2 GHz LNA with 15.8 dBm IIP3, 18 dB gain, 1.15 dB noise figure, and a |s11| less than -20 dB for a biasing current of 7.5 mA. The calculated results show good agreement with HP Advanced-Design-System simulations. The design tradeoffs illuminated by this optimization methodology are highlighted and discussed.

❑ Return to main document.